普誠科技股份有限公司
Princeton Technology Corp.
Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

DESCRIPTION

PT2258 is a 6-Channel Electronic Volume Controller IC utilizing CMOS Technology specially designed for the new generation of AV Multi-Channel Audio System. PT2258 provides an I^2C Control Interface, an attenuation range of 0 to -79dB at 1dB/step, low noise, and high channel separation. Housed in 20 pins, DIP or SOP, PT2258's pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

FEATURES

- CMOS Technology
- Low Power Consumption
- Least External Components
- Attenuation Range: 0 to -79dB at 1dB/step
- Operating Voltage: 5 to 9 V
- Low Noise, S/N Ratio>100dB (A-weighting)
- High Channel Separation
- I^2C Bus Control Interface
- Selectable Address
- 6-Channel Outputs
- Available in 20 pins, DIP or SOP

APPLICATIONS

- AV Surround Audio Equipment
- Car Audio
- Mini Compo
- Computer Multi-Media Speaker
- Other Audio Equipments

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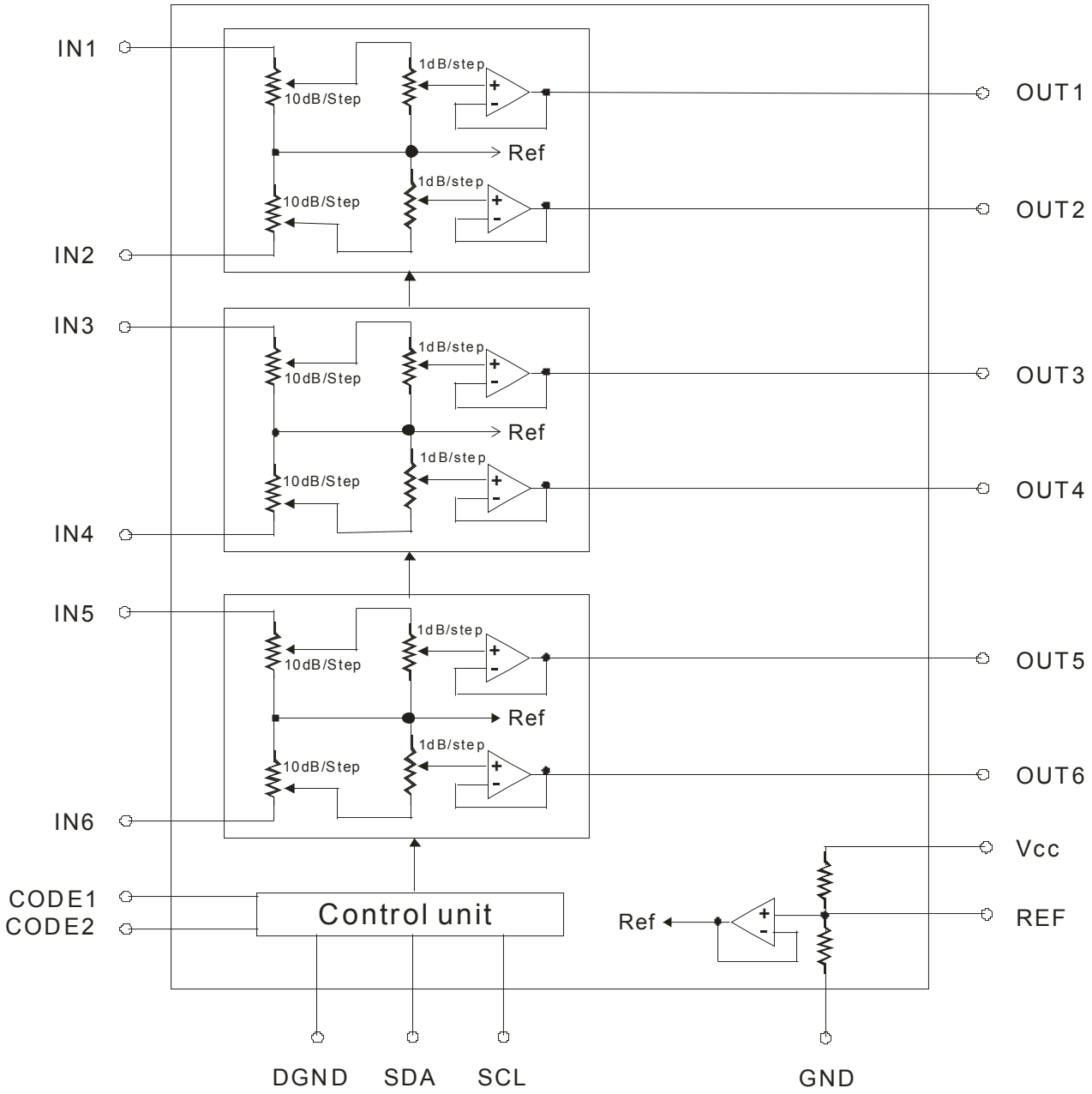
BLOCK DIAGRAM



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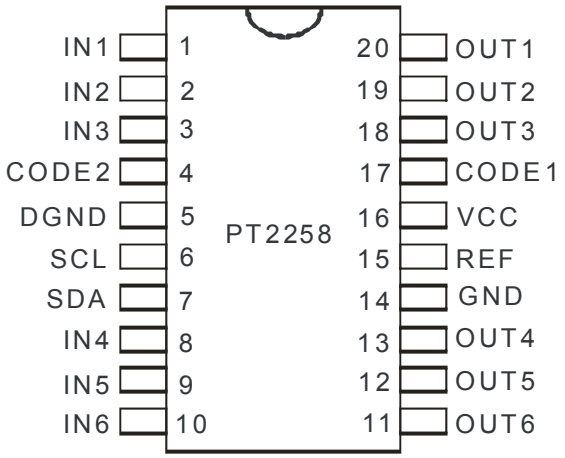
PIN CONFIGURATION



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PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
IN1	I	Channel Input No. 1. Connect a Capacitor to Audio Source	1
IN2	I	Channel Input No. 2 Connect a Capacitor to Audio Source	2
IN3	I	Channel Input No. 3 Connect a Capacitor to Audio Source	3
CODE2	-	Refer to Address Code Section	4
DGND	-	Digital Ground	5
SCL	I	I^2C Clock Input	6
SDA	I	I^2C Data Input	7
IN4	I	Channel Input No. 4 Connect a Capacitor to Audio Source	8
IN5	I	Channel Input No. 5 Connect a Capacitor to Audio Source	9
IN6	I	Channel Input No. 6 Connect a Capacitor to Audio Source	10
OUT6	O	Channel Output No. 6 Connect a Capacitor to the Next Stage	11
OUT5	O	Channel Output No. 5 Connect a Capacitor to the Next Stage	12
OUT4	O	Channel Output No. 4 Connect a Capacitor to the Next Stage	13
GND	-	Ground 14	14
REF	-	Reference Voltage= 1/2 Vcc Connect a Capacitor to the Ground	15
VCC	-	Power Supply Input 16	16
CODE1	-	Refer to the Address Code Section	17
OUT3	O	Channel Output No. 3 Connect a Capacitor to the Next Stage	18
OUT2	O	Channel Output No. 2 Connect a Capacitor to the Next Stage	19
OUT1	O	Channel Output No. 1 Connect a Capacitor to the Next Stage	20

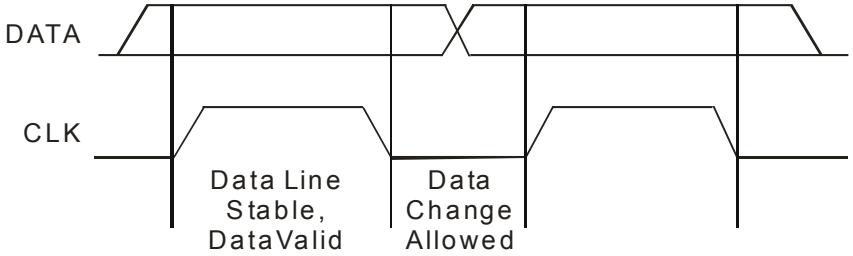
FUNCTION DESCRIPTION

BUS INTERFACE

Data are transmitted to and from the microprocessor to the PT2258 via the SDA and SCL. The SDA and SCL make up the BUS Interface. It should be noted that the pull-up resistors must be connected to the positive supply voltage.

DATA VALIDITY

A data on the SDA Line is considered valid and stable only when the SCL Signal is in HIGH State. The HIGH and LOW States of the SDA Line can only change when the SCL signal is LOW. Please refer to the figure below.

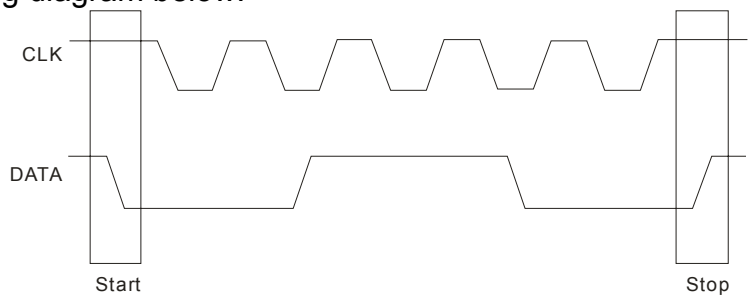


START AND STOP CONDITIONS

A Start Condition is activated when
1. the SCL is set to HIGH and
2. SDA shifts from HIGH to LOW State.

The Stop Condition is activated when
1. SCL is set to HIGH and
2. SDA shifts from LOW to HIGH State.

Please refer to the timing diagram below.

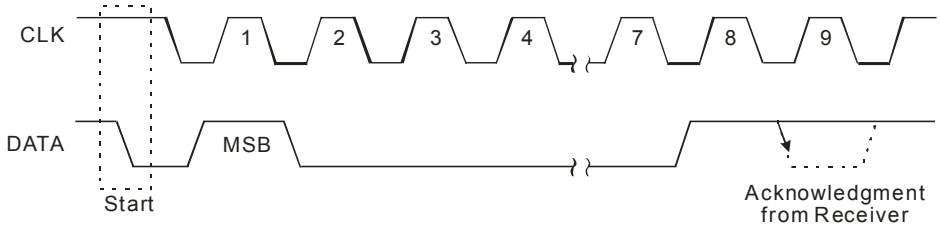


BYTE FORMAT

Every byte transmitted to the SDA Line consists of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is transmitted first.

ACKNOWLEDGE

During the Acknowledge Clock Pulse, the master (μP) puts a resistive HIGH level on the SDA Line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during the Acknowledge Clock Pulse so that the SDA Line is in a Stable Low State during this Clock Pulse. Please refer to the diagram below.
The audio processor that has been addressed has to generate an Acknowledge after receiving each byte, otherwise, the SDA Line will remain at the High Level during the ninth (9th) Clock Pulse. In this case, the master transmitter can generate the STOP Information in order to abort the transfer.



TRANSMISSION WITHOUT ACKNOWLEDGE

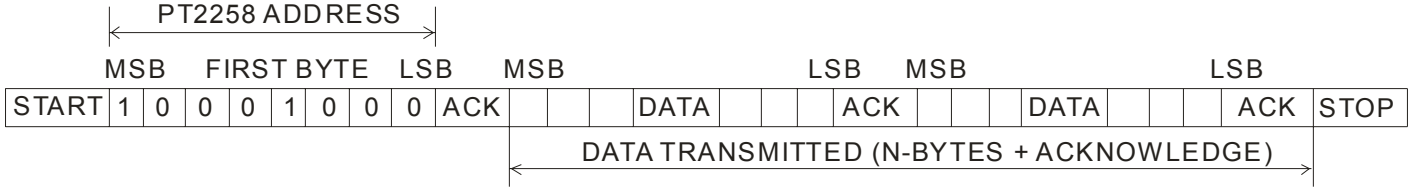
If you want to avoid the acknowledge detection of the audio processor, a simpler μP transmission may be used. Wait one clock and do not check the slave acknowledge of this same clock then send the new data. If you use this approach, there are greater chances of faulty operation as well as decrease in noise immunity.

INTERFACE PROTOCOL

The interface protocol consists of the following:

- A Start bit
- A Chip Address Byte
- ACK=Acknowledge bit
- A Data byte
- A Stop bit

Please refer to the diagram below:



Notes:
1. ACK=Acknowledge
2. Max. Clock Speed=100K Bits/s

PT2258 ADDRESS CODE

PT2258 Address Code depends on the state of CODE1 (Pin No.17) and CODE2 (Pin No.4).

If CODE1 or CODE2 is connected to Vcc, then CODE1 or CODE2 is set to “1”. If CODE1 or CODE2 is connected to the Ground, it is set to “0”. Please refer to the information below:

Condition 1:

CODE1	CODE2
1	1

Then, PT2258 Address Code is 8 CH:

1 MSB	0	0	0	1	1	0	0 LSB

Condition 2:

CODE1	CODE2
1	0

Then, PT2258 Address Code is 88 H:

1 MSB	0	0	0	1	0	0	0 LSB

Condition 3:

CODE1	CODE2
0	1

Then, PT2258 Address Code is 84 H:

1 MSB	0	0	0	0	1	0	0 LSB

Condition 4:

CODE1	CODE2
0	0

Then, PT2258 Address Code is 80H:

1 MSB	0	0	0	0	0	0	0 LSB

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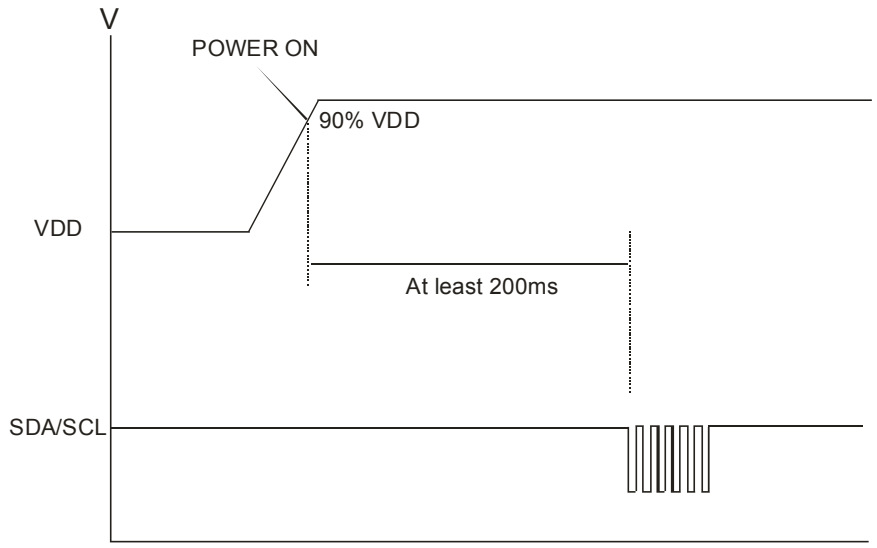
I²C BUS INTERFACE START TIME

After Power is turned ON, PT2258 needs to wait for a short time in order to insure stability. The waiting time period for PT2258 to send I²C Bus Signal is at least 200ms. If the waiting time period is less than 200ms, I²C Control may fail. Please refer to the diagram below.



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PT2258 CONTROL SOFTWARE PROCEDURE

1. In order to ensure exact operation under any operating voltage, it is recommended an instruction to clear the register “C0H” must be transmitted first. Please refer to the following diagram:

Start	1	0	0	0	1	0	0	0	Ack	1	1	0	0	0	0	0	0	Ack	Stop
		2258 Address									Clear Register								

2. The PT2258 function register does not have any default settings. After clearing the register, an initial value must send in order to each register. If a register does has not been set, it is possible that no sound will be output.

3. When adjusting the volume of PT2258, it is necessary to send a multiple of 10dB followed by a 1dB code to the attenuator in sequence. If this sequence is not followed, or if only a 10dB or 1dB value is sent, the IC may not operate normally. Please refer to the diagram below:

Volume setting -42dB：

Start	1	0	0	0	1	0	0	0	Ack	1	1	0	1	0	1	0	0	ACK	1	1	1	0	0	0	1	0	Ack	Stop
		PT2258 Address												-40dB										-2dB				

Start	1	0	0	0	1	0	0	0	Ack	1	1	1	0	0	0	1	0	Ack	1	1	0	1	0	1	0	0	ACK	Stop
		PT2258 Address												-2dB										-40dB				

The two methods above are both acceptable.

Warning!! The following transmission method is not permitted.

Send only a 10dB attenuation value:

Start	1	0	0	0	1	0	0	0	Ack	1	1	0	1	0	1	0	0	ACK	Stop
		PT2258 Address									-40dB								

Send only a 10dB attenuation value:

Start	1	0	0	0	1	0	0	0	Ack	1	1	1	0	0	0	1	0	ACK	Stop
		PT2258 Address									-2dB								

Do not send a 10dB code without simultaneously with a 1dB code or in combination with other instruction codes.

Start	1	0	0	0	1	0	0	0	Ack	1	1	1	0	0	0	1	0	Ack	1	1	1	1	1	0	0	1	ACK	1	1	0	1	0	1	0	0	ACK	Stop
		PT2258 Address												-2dB														All CH mute									-40dB	

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DATA BYTES DESCRIPTION

FUNCTION BITS

MSB							LSB	FUNCTION
1	1	1	0	A3	A2	A1	A0	6-Channel, -1dB/step
1	1	0	1	0	B2	B1	B0	6-Channel, -10dB/step
0	0	0	1	A3	A2	A1	A0	Channel No. 3, -1dB/step
0	0	0	0	0	B2	B1	B0	Channel No. 3, -10dB/step
0	0	1	1	A3	A2	A1	A0	Channel No. 4, -1dB/step
0	0	1	0	0	B2	B1	B0	Channel No. 4, -10dB/step
0	1	0	1	A3	A2	A1	A0	Channel No. 2, -1dB/step
0	1	0	0	0	B2	B1	B0	Channel No. 2, -10dB/step
0	1	1	1	A3	A2	A1	A0	Channel No. 5, -1dB/step
0	1	1	0	0	B2	B1	B0	Channel No. 5, -10dB/step
1	0	0	1	A3	A2	A1	A0	Channel No. 1, -1dB/step
1	0	0	0	0	B2	B1	B0	Channel No. 1, -10dB/step
1	0	1	1	A3	A2	A1	A0	Channel No. 6, -1dB/step
1	0	1	0	0	B2	B1	B0	Channel No. 6, -10dB/step
1	1	1	1	1	0	0	M	6-Channel, Mute When M= 1, Mute On When M=0, Mute Off

ATTENUATION UNIT BIT

A3/---	A2/B2	A1/B1	A0/B0	Attenuation Value(dB)
0	0	0	0	0/0
0	0	0	1	-1/-10
0	0	1	0	-2/-20
0	0	1	1	-3/-30
0	1	0	0	-4/-40
0	1	0	1	-5/-50
0	1	1	0	-6/-60
0	1	1	1	-7/-70
1	0	0	0	-8/-
1	0	0	1	-9/-

Note: Ax=-1dB/step, Bx=-10dB/step

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ABSOLUTE MAXIMUM RATINGS

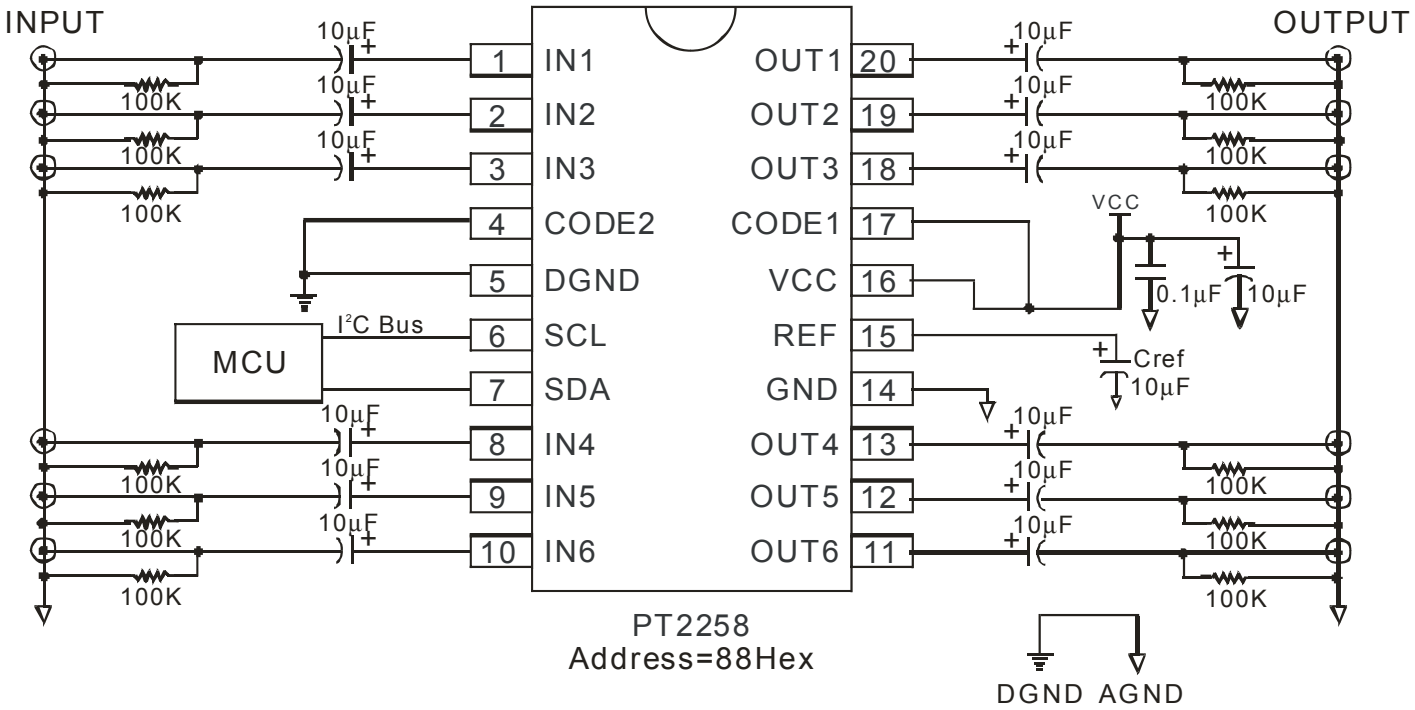
Parameter	Symbol	Ratings	Unit
Supply Voltage	Vs	12	V
Operation Temperature	Topr	-40～+85	℃
Storage Temperature	Tstg	-65～+150	℃

ELECTRICAL CHARACTERISTICS

(V_{DD}=9V, V_I=1Vrms, f=1KHz, Temp=27℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}		5	9	10	V
Supply Current	Is		7	10	12	mA
Input Impedance	R_{IN}	FL, FR, CTR, SUB, SL, SR	22	33	42	KΩ
Max. Input Voltage	V_{CL}	Volume=0dB, THD=1%	-	2.8	3.0	Vrms
Channel Separation	Sc		90	100	110	dB
Volume Control Range	Crange		-	79	-	dB
Max. Attenuation	Avmax		-	-79	-	dB
Attenuation Step	Astep		-	1	-	dB
Attenuation Error	EA	Volume=0～-50dB	-1.0	0	+1.0	dB
Mute Attenuation	AMUTE	A-weighting	90	95	98	dB
Total Harmonic Distortion	THD	Volume=0dB, input 200mVrms	0.003	0.005	0.01	%
Output Noise	Noise	A-weighting	-	3	5	μV
Signal-Noise Ratio	S/N	0dB=1Vrms, A-weighting	100	105	110	dB
Output Impedance	Ro		-	600	900	Ω
Output Gain	Go		-0.5	0	+0.5	dB
Max. Output Voltage	Vomax	FL, FR, CENTER, SUB, SL, SR THD=1%	2.3	2.5	2.8	Vrms
I^2C Section						
Bus Low Input Level	V_{IL}		0	2.4	2.5	V
Bus High Input Level	V_{IH}		2.8	3.0	V_{DD}	V
Bus Initialization	T_{INIT}	Cref=10μF	-	250	300	mS

APPLICATION CIRCUIT



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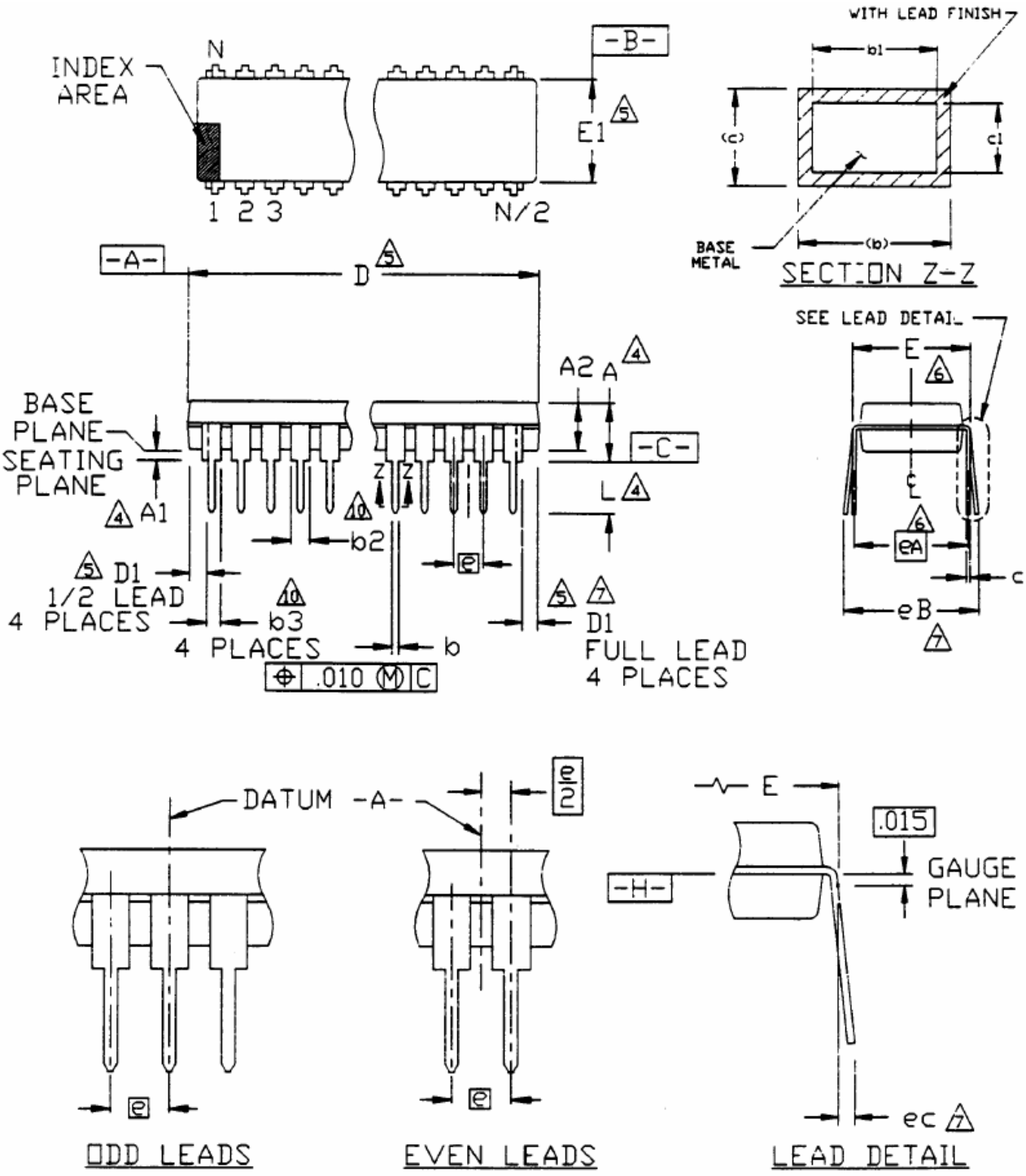
ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2258	20 Pins, DIP, 300mil	PT2258
PT2258-S	20 Pins, SOP, 300mil	PT2258-S
PT2258 (L)	20 Pins, DIP, 300mil	PT2258
PT2258-S (L)	20 Pins, SOP, 300mil	PT2258-S

Notes:
1. (L), (C) or (S) = Lead Free
2. The Lead Free mark is put in front of the date code.

PACKAGE INFORMATION

20 PINS, DIP, 300MIL



Symbol	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.980	1.030	1.060
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	-	0.100 bsc.	-
eA	-	0.300 bsc.	-
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes:
1. All dimensions are in INCHES.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension ”A”, ”A1” and ”L” are measured with the package seated in JEDEC Seating Plane Gauge GS-3
4. “D”, ”D1” and “E1” dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
5. “E” and “eA” measured with the leads constrained to be perpendicular to datum -C- .
6. “eB” and “eC” are measured at the lead tips with the leads unconstrained.
7. N is the number of the terminal positions (N=20)
8. Pointed or rounded lead tips are preferred to ease insertion.
9. “b2” and “b3” maximum dimensions are not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm)
10. Distance between leads including dambar protrusions to be 0.005 inch minimum.
11. Datum plane -H- coincident with the bottom of lead, where lead exits body.
12. Refer to JEDEC MS-001, Variation AD.

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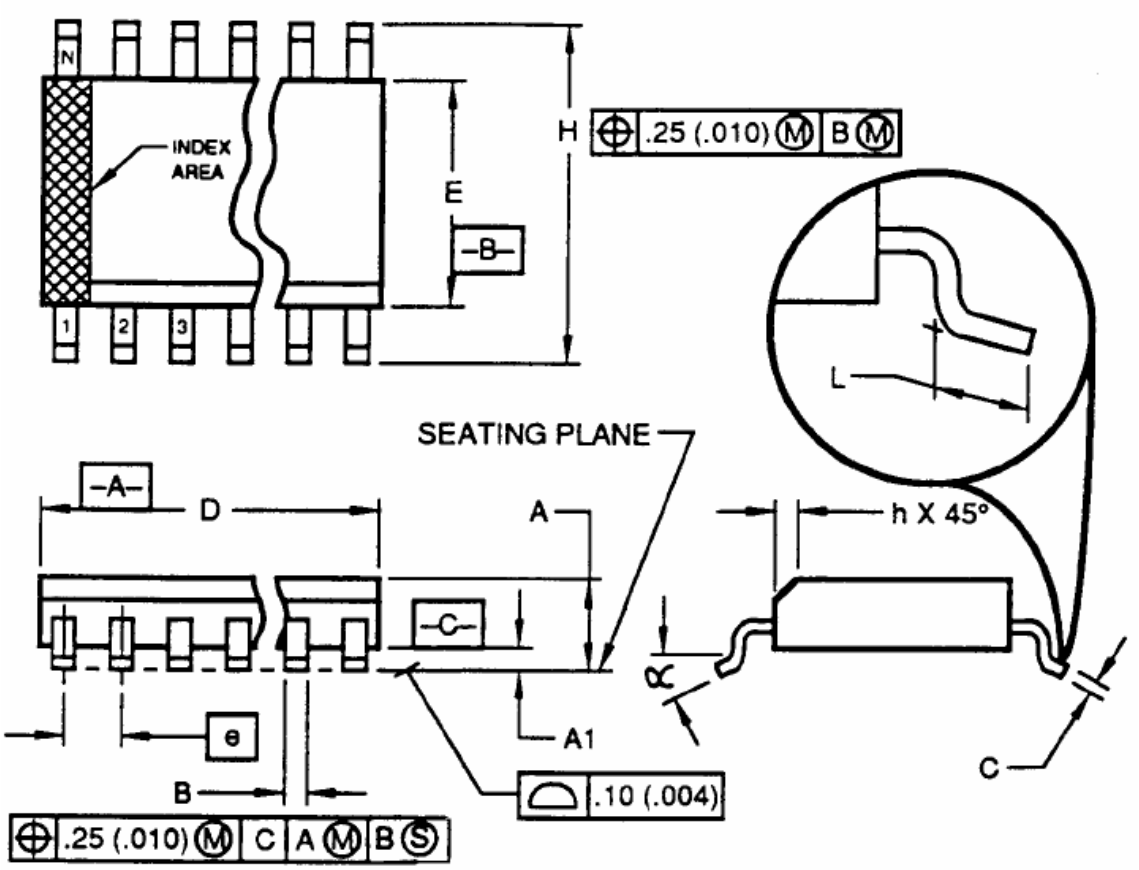
20 PINS, SOP, 300MIL



Symbol	Min.	Nom.	Max.
A	2.35	-	2.65
A1	0.10	-	0.30
B	0.33	-	0.51
C	0.23	-	0.32
D	12.60	-	13.00
E	7.40	-	7.60
e	-	1.27 bsc.	-
H	10.00	-	10.65
h	0.25	-	0.75
L	0.40	-	1.27
α	0°	-	8°

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension “E” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. “L” is the length of the terminal for soldering to a substrate.
6. N is the number of the terminal positions (N=20)
7. The lead width “B” as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in).
8. Controlling dimension: MILLIMETER.
9. Refer to JEDEC MS-013, Variation AC.

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